Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths, comprising the steps of:
(a)determining for each one of the plurality of timing paths a corresponding delay; and
(b)inserting a delay element into each one of the plurality of timing paths having said corresponding delay, said delay element configured to induce said corresponding delay into that one of the plurality of timing paths.

[c2] 2. A method according to claim 1, wherein at least some of the plurality of timing paths each have early mode problems, the method further comprising, prior to step (b), the step of fixing said early mode problems.

[c3] 3. A method according to claim 1, wherein each one of the plurality of timing paths has a corresponding late mode margin and step (a) includes setting each said corresponding delay to said corresponding late mode margin.

[c4] 4. A method according to claim 3, wherein the overall in-

stantaneous current draw has a profile and step (a) includes setting each one of at least some of said corresponding delays to said corresponding late mode margin minus a fraction of the timing cycle.

[c5] 5. A method according to claim 4, wherein at least some of the plurality of timing paths each have early mode problems, the method further comprising, following step (a), the step of fixing said early mode problems

[c6] 6. A method according to claim 3, wherein each one of the plurality of timing paths has a corresponding early mode margin and step (a) includes setting each corresponding delay to said corresponding late mode margin minus said corresponding early mode margin.

[c7] 7. A method according to claim 6, wherein the overall instantaneous current draw has a profile and step (a) includes setting each one of at least some of said corresponding delays to said corresponding late mode margin minus a fraction of the timing cycle.

[c8] 8. A method according to claim 7, wherein at least some of the plurality of timing paths each have at least one early mode problem, the method further comprising, following step (a), the step of fixing said early mode problems.

[c9] 9. A method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths each having a late mode margin, comprising the steps of:

(a)determining if the late mode margin of each one of the plurality of timing paths is greater than zero; and

(b)for each one of the plurality of timing paths having a late mode margin greater than zero, determining a delay for that one of the plurality of timing paths, said delay being a function of the corresponding late mode margin.

[c10] 10. A method according to claim 9, wherein each said delay is equal to the corresponding late mode margin.

[c11] 11. A method according to claim 9, wherein the overall instantaneous current draw has a profile having a peak defined by a portion of the plurality of timing paths, the method further comprising the step of removing at least one timing path from said portion of the plurality of timing paths.

[c12] 12. A method according to claim 9, wherein at least some of the plurality of timing paths each have at least one early mode problem, the method further comprising the step of fixing each one of said late mode problems.

[c13] 13. A method according to claim 9, wherein the overall instantaneous current draw has a profile having a peak defined by a portion of the plurality of timing paths, the method further comprising the step of removing at least one timing path from said portion of the plurality of timing paths.

[c14] 14. A method according to claim 9, wherein the plurality of timing paths each have an early mode margin, the method further comprising the step of, for each one of the timing paths having a late mode margin greater than zero and an early mode margin greater than zero, subtracting the early mode margin from the late mode margin.

[c15] 15. A method according to claim 14, wherein the overall instantaneous current draw has a profile having a peak defined by a portion of the plurality of timing paths, the method further comprising the step of removing at least one timing path from said portion of the plurality of timing paths.

[c16] 16. An integrated circuit, comprising:
(a)a plurality of timing paths each having a late mode margin;
(b)a delay element located in each one of at least some

of said plurality of timing paths, each of said delay elements having a delay that is a function of said late mode margin of the corresponding one of said plurality of timing paths.

[c17] 17. An integrated circuit according to claim 16, wherein each said delay is substantially equal to said late mode margin of the corresponding one of said plurality of timing paths.

[c18] 18. An integrated circuit according to claim 16, wherein at least one said delay is substantially equal to said late mode margin of the corresponding one of said plurality of timing paths minus a predetermined period.

[c19] 19. An integrated circuit according to claim 16, wherein said plurality of timing paths each have an early mode margin and each said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths.

[c20] 20. An integrated circuit according to claim 16, wherein at least one said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths minus a predetermined period.